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[54] **ENHANCED PLANARIZATION TECHNIQUE FOR AN INTEGRATED CIRCUIT**

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[21] Appl. No.: **09/007,668**

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Related U.S. Application Data

[63] Continuation of application No. 08/456,343, Jun. 1, 1995, abandoned, which is a continuation of application No. 08/163,043, Dec. 6, 1993, Pat. No. 5,435,888.

[51] **Int. Cl.**[6] **H01L 23/58**

[52] **U.S. Cl.** **257/644**; 257/647; 257/634

[58] **Field of Search** 257/644, 647, 257/634

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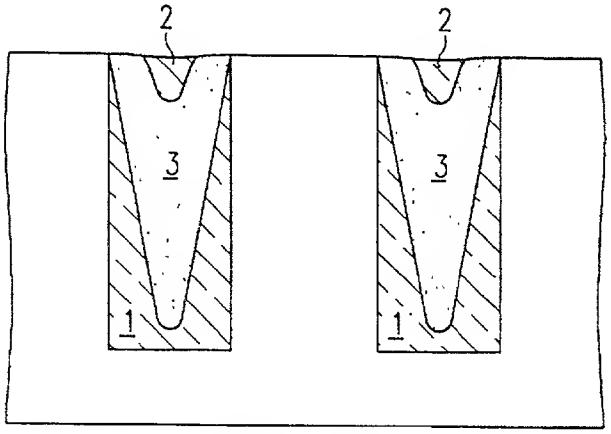
[57] **ABSTRACT**

A method for planarizing integrated circuit topographies, wherein, after a first layer of spin-on glass is deposited, a layer of low-temperature oxide is deposited before a second layer of spin-on glass.

22 Claims, 4 Drawing Sheets



SOG/LTO etchback

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